



# NXP ultra-low power L1 GPS RFIC GNR1040

## Ultra-low power, high-performance GPS RF front-end

Optimized for high performance, ultra-low power, low cost, and small form factor, this highly integrated GPS solution is easy to implement and fully programmable.

### Key features

- ▶ Optimized for cellular handset integration
- ▶ Excellent linearity, noise-figure, and phase-noise specifications
- ▶ Built-in flexibility to support multiple GPS baseband processors
- ▶ Ultra-low power consumption (15 mW)
- ▶ 1.8-V supply voltage
- ▶ Integrated LNA with on-chip matching network
- ▶ Fully integrated IF filtering (no external IF components)
- ▶ Integrated fractional-N PLL and VCO
- ▶ On-chip crystal oscillator circuit
- ▶ Supports all cellular-handset reference frequencies (10 to 50 MHz)
- ▶ Flexible quantization (1- or 2-bit) and data interface
- ▶ SPI control interface
- ▶ Power-down and standby modes
- ▶ Very low external component count
- ▶ Operating temperature range: -40 to +85 °C
- ▶ 24-pin QFN package (4 x 4 mm)

### Applications

- ▶ Cellular handset integration for E911, navigation, and location-based services
- ▶ Handheld consumer navigation and multifunction devices
- ▶ Battery-operated GPS devices

The NXP GNR1040 is a highly integrated, low-power, GPS RFIC operating in the 1.575-GHz (L1) signal band. It is based on a single-conversion-to-low-IF architecture, with fully integrated IF filtering, and is designed in a leading-edge SiGe BiCMOS process.

It has excellent specifications for linearity, noise figure, and phase noise.

Its high-resolution, fractional-N synthesizer supports the use of a wide range of external reference frequencies or crystals.

Only a handful of components are required to create a complete, low-cost, small form-factor GPS RF front-end design.

There is a fully integrated GPS receive path, with a low noise amplifier (LNA), that down-converts the GPS L1 signal (1575.42 MHz) to a 4-MHz IF. The signal can be quantized to one or two bits and delivered through a programmable streaming data interface to GPS baseband devices.

The fractional-N frequency synthesizer architecture can use any clock reference frequency in the range of 10 to 50 MHz, enabling the support of all common reference frequencies used in cellular handsets.

A standard SPI interface allows access to the internal register bank. This enables optimization of the various programmable parameters under software control, for specific GPS system implementations.

NXP supports the GNR1040 with flexible evaluation kits and reference designs, including a PC-based tool for controlling the device's parameters, simplifying the evaluation and integration of the device.

Block diagram of GNR1040

